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Christopher Hoover

Summary of qualifications

Systems engineer with a deep understanding of business and of hardware and software systems and applications.

Objective

Senior technologist position leading advanced research and development alongside a highly competent team.

Education

1990 Carnegie-Mellon University Pittsburgh, PA

B.S. Computer Engineering

- Honors
- Alumnus, Center for Silicon System Implementation

Professional experience

2000-present **Hewlett-Packard Laboratories** Palo Alto, CA

Research Scientist/Engineer

- Collaborated with Berkeley Wireless Research Center (BWRC) on ultra-low power radio architectures and radio systems.
- Implemented multiple devices for the Agile Computing effort and developed the network discovery and transport layers.
- Created a Bluetooth-based wireless picture frame that worked particularly well with existing mobile phones.
- Led a multi-disciplinary team to develop a "remote" camera. This novel imaging device had interesting social applications and fit well in the market between digital still cameras and camera phones.
- Architected systems and applications of digital "datacasting" that piggybacked synchronous and asynchronous digital data delivery with legacy analog and digital television broadcasts. Developed business models for both developed and developing markets.
- Presently involved in research and development of advanced storage system architectures for cost-effective, long-term (>50 years) preservation of digital assets.

1999-2000 **OneSpot** Santa Clara, CA

Founder and CTO

- Architected and implemented a multi-tiered web and messaging infrastructure.
- Ran operations and managed all vendor relationships.
- In the same timeframe, wrote business plan and raised money for another venture providing outsourced messaging for small and medium businesses.

1990-1999 **Cadence Design Systems** San Jose, CA

Architect

- Chief Architect on Virtual Component Co-Design (VCC), a hardware-software co-design platform developed in partnership with several major semiconductor and system companies. Liaison to key partners including Ericsson, Intel and National Semiconductor on VCC and BONeS. Worked closely with sales to support these accounts.
- Principal Engineer in Systems & Networks, Inc., a spin-out of Cadence. Responsible for network design and capacity planning simulation tools and for new product development.
- Key designer and developer of Block Oriented Network Simulator (BONeS), a popular discrete event simulation tool aimed at network design and network protocol development.

1986-1990 **Carnegie-Mellon University** Pittsburgh, PA

Developer

- Implementer of CMU Common Lisp. Designed and implemented an efficient garbage collector, designed and implemented operating system adapting layer, performed several ports, and implemented several compiler back-ends (MIPS, PA-RISC, 68K). This implementation is available today in the Debian Linux distribution and elsewhere.

Patents and publications

US 6,882,965 Method for Hierarchical Specification of Scheduling in System-level Simulations

WO0227565 Performance Level Modeling and Simulation of Electronic Systems Having Both Hardware and Software

Five patents pending with Hewlett-Packard Company.

Instruction-Level Parallelism and Parallelizing Compilation, 1991, Schloss Dagstuhl International Conference and Research Center for Computer Science

References

Upon request